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EXAMINER	
NGUYEN, STEVE N	
ART UNIT	**PAPER NUMBER**
2138	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,793	ZORIAN ET AL.	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 have been examined.

Drawings

2. The drawings are objected to because they contain handwritten reference numbers. The drawings also fail to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description on page 13, paragraph 23: 302-332. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 34 and 38 are objected to. Claim 37 objected to because of the following informalities: claim 34 recites, "the machine-readable medium of claim 32". However, claim 32 is not a machine-readable medium. Claim 38 should end with a period. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5, 7, 13, 15, 20, 26 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites, "wherein a fuse is a non-volatile storage device that performs the function of a fuse". There is a lack of antecedent basis for "a fuse".

Claim 7 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. Claim 7 recites, "wherein the processor further includes logic configured to decompress an amount of bits making up the actual repair signature". The omitted elements are: a data compressor.

Claim 13 recites the term "compression/decompression logic". It is unclear whether "compression/decompression logic" is both compression logic and

decompression logic; of whether "compression/decompression logic" is either compression logic or decompression logic.

Claim 15 recites, "a second processor containing redundancy allocation logic and coupled to one or more memories, wherein the repair data container to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor". There is a lack of antecedent basis for "the first processor". Furthermore, the recitation, "wherein the repair data container to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor" contains grammatical errors. It is unclear whether the repair data container repairs the memories connected the first processor as well as the memories connected to the second processor, or whether a concatenated repair signature repairs the memories connected the first processor as well as the memories connected to the second processor.

Claim 20 recites, "wherein the first processor also includes logic configured to test the memories in the field to augment the concatenated repair signature stored in the repair data container." There is a lack of antecedent basis for "the field".

Claim 26 recites, "wherein the processors and the fuse box are embedded on a single chip". There is a lack of antecedent basis for "the fuse box" and "the processors". It is assumed that applicant intended claim 26 to depend from claim 22 instead of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 27, 29, 30, and 32 rejected under 35 U.S.C. 102(e) as being anticipated by Anand et al (US Pat. 6,577,156; hereinafter referred to as Anand).

As per claim 27:

Anand teaches a method, comprising:

- composing a repair signature for two or more memories (col. 5, lines 3-20);
- sending the repair signature to be stored in non-volatile fuses (col. 3, lines 51-54); and
- decompressing the repair signature to send reconfiguration data to the two or more memories (col. 3, lines 54-58).

As per claim 29:

Anand teaches the method of claim of 27, further comprising: repairing an adjustable subset of memories having redundant elements (abstract).

As per claim 30:

Anand teaches an apparatus, comprising:

- means for composing a repair signature for two or more memories (col. 5, lines 3-20);
- means for sending the repair signature to be stored in non-volatile fuses (col. 3, lines 51-54); and
- means for decompressing the repair signature to send reconfiguration data to the two or more memories (col. 3, lines 54-58).

As per claim 32:

Anand teaches the apparatus of claim of 30, further comprising: means for repairing an adjustable subset of memories having redundant elements (abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-21, 27, 28, 30, 31, 35, and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss et al (US Pat. 6,249,465; hereinafter referred to as Weiss) in view of Anand et al (US Pat. 6,577,156; hereinafter referred to as Anand).

As per claim 1:

Weiss teaches an apparatus, comprising:

- two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells (Fig. 6, elements 700-715);
- a processor containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each memory (col. 16, lines 12-20).

Not explicitly disclosed by Weiss is a repair data container to store an actual repair signature for each memory having one or more defective memory cells detected during fault testing and a dummy repair signature for each memory with no defective memory cells. However, Anand in an analogous art teaches a repair data container (Fig. 1, element 11), and Weiss teaches elements designed to store an actual repair signature for each memory having one or more defective memory cells detected during fault testing (col. 11, lines 26-33) and a dummy repair signature for each memory with no defective memory cells (col. 11, lines 43-46).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the elements of Weiss shown in Fig. 6 into a repair data container such as the one disclosed by Anand. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made,

because it has been held that integrating together a plurality of pieces involves only routine skill in the art. *In re Larson* 144 USPQ 347 (CCPA 1965).

As per claim 2:

Weiss teaches the apparatus of claim 1, wherein the repair data container storing the repair signature for each memory is a fuse box located external to a memory block (Fig. 6, element 610).

As per claim 3:

Weiss teaches the apparatus of claim 1, wherein the dummy repair signature for each memory with no defect is an identifier bit directing the processor to bypass loading of reconfiguration data into the memory corresponding to this identifier bit (col. 11, lines 43-46).

As per claim 4:

Weiss teaches the apparatus of claim 1, wherein the dummy repair signature for each memory with no defect is an identifier bit directing the processor to load a prestored series of reconfiguration data bits into scan chain registers of the memory corresponding to this identifier bit but the content of the reconfiguration data bits does not cause a substitution of a redundant component for a non-redundant component in that memory (col. 11, lines 43-46).

As per claim 5:

Weiss teaches the apparatus of claim 1, wherein a fuse is a non-volatile storage device that performs the function of a fuse (col. 9, lines 25-30).

As per claim 6:

Anand teaches the apparatus of claim 1, wherein the processor further includes logic configured to compress an amount of bits making up the actual repair signature (col. 3, lines 51-54).

As per claim 7:

Anand teaches the apparatus of claim 1, wherein the processor further includes logic configured to decompress an amount of bits making up the actual repair signature (col. 3, lines 51-54).

As per claim 8:

Anand teaches the apparatus of claim 1, wherein the processor further includes logic configured to compose a concatenated repair signature for all of the memories sharing a fuse box (col. 3, lines 54-58).

As per claim 9:

Weiss teaches the apparatus of claim 1, wherein the repair data container contains an amount of fuses to store actual repair signatures for an adjustable subset of the redundant components associated with the two or more memories and dummy repair signatures for the remaining memories (col. 9, lines 36-38).

As per claim 10:

Weiss teaches the apparatus of claim 1, wherein the repair data container stores indicator bits for each memory sharing that repair data container, and a presence of an active bit in the indicator bits indicates that the repair data container contains an actual repair signature for that memory having a defect (col. 5, lines 1-7).

As per claim 11:

Weiss teaches the apparatus of claim 2, wherein the fuse box has a dedicated field for each memory sharing that fuse box, and a presence of an active bit in the dedicated field indicates that the fuse box contains an actual repair signature for that memory having a defect (col. 11, lines 5-9).

As per claim 12:

Weiss teaches the apparatus of claim 1, wherein the processor further includes logic configured to provide built in self-test logic, built-in self-diagnosis logic, and reconfiguration data logic (col. 13, lines 46-49).

As per claim 13:

Anand teaches the apparatus of claim 1, further comprising compression/decompression logic around the repair data container configured to compress an amount of bits making up a repair signature and decompress an amount of bits making up a repair signature (Fig. 1, element 14).

As per claim 14:

Weiss teaches the apparatus of claim 1, wherein the processor, repair data container, and the memories are embedded on a single chip (col. 1, lines 55-58).

As per claim 15:

Anand teaches the apparatus of claim 1, further comprising: a second processor containing redundancy allocation logic and coupled to one or more memories, wherein the repair data container to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor (col. 3, line 67-col. 4, line 2).

As per claim 16:

Weiss teaches an apparatus, comprising:

- two or more memories having redundant components that share the repair data container (Fig. 6, elements 700-715), wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the two or more memories (col. 9, lines 36-38).

Not explicitly disclosed by Weiss is a repair data container located on a chip, the repair data container to store an actual repair signature far each memory having a defective memory cell. However, Anand in an analogous art teaches a repair data container (Fig. 1, element 11), and Weiss teaches elements designed to store an actual repair signature for the memories (col. 11, lines 26-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the elements of Weiss shown in Fig. 6 into a repair data container such as the one disclosed by Anand. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because it has been held that integrating together a plurality of pieces involves only routine skill in the art. *In re Larson* 144 USPQ 347 (CCPA 1965).

As per claim 17:

Weiss teaches the apparatus of claim 16, wherein the repair data container also stores dummy repair signatures for each memory with no defective memory cells (col. 11, lines 43-46).

As per claim 18:

Weiss teaches the apparatus of claim 17, further comprising: a processor containing redundancy allocation logic and coupled to the repair data container, wherein the repair data container to store a concatenated repair signature that includes the actual repair signatures and the dummy repair signatures (col. 11, lines 38-46).

As per claim 19:

Anand teaches the apparatus of claim 17, further comprising: a first processor coupled to the repair data container, wherein the first processor contains logic configured to decompress an amount of bits making up the actual repair signatures (Fig. 1, element 14).

As per claim 20:

Anand teaches the apparatus of claim 19, wherein the first processor also includes logic configured to test the memories in the field to augment the concatenated repair signature stored in the repair data container (col. 3, lines 51-54).

As per claim 21:

Anand teaches the apparatus of claim 19, further comprising: a second processor containing logic configured to test and repair memories connected to the second processor; wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the memories connected to the second processor as well as memories connected to the first processor (col. 3, line 67-col. 4, line 2).

As per claims 27 and 28:

Weiss teaches a method, comprising:

- composing a repair signature for two or more memories (col. 11, lines 26-33);
- sending the repair signature to be stored in non-volatile fuses (col. 11, lines 26-33);
- storing an actual repair signature for a subset of the two or memories (col. 11, lines 26-33) and a dummy repair signature for the remaining memories (col. 11, lines 43-46).

Not explicitly disclosed by Weiss is decompressing the repair signature to send reconfiguration data to the two or more memories. However, Anand in an analogous art teaches decompressing data in a fuse box (col. 3, lines 54-58). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the decompressor of Anand with the circuit of Weiss. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that a compressor and decompressor would have saved space.

As per claims 30 and 31:

Weiss teaches an apparatus, comprising:

- means for composing a repair signature for two or more memories (col. 11, lines 26-33);
- means for sending the repair signature to be stored in non-volatile fuses (col. 11, lines 26-33); and

- means for storing an actual repair signature for a subset of the two or memories (col. 11, lines 26-33) and a dummy repair signature for the remaining memories (col. 11, lines 43-46).

Not explicitly disclosed by Weiss is means for decompressing the repair signature to send reconfiguration data to the two or more memories. However, Anand in an analogous art teaches decompressing data in a fuse box (col. 3, lines 54-58). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the decompressor of Anand with the circuit of Weiss. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that a compressor and decompressor would have saved space.

As per claim 35:

Weiss teaches a machine readable medium that stores data representing an integrated circuit, comprising:

- two or more memories having redundant components that share the repair data container (Fig. 6, elements 700-715), wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the two or more memories (col. 9, lines 36-38).

Not explicitly disclosed by Weiss is a repair data container located on a chip, the repair data container to store an actual repair signature for each memory having a defect. However, Anand in an analogous art teaches a repair data container (Fig. 1,

element 11), and Weiss teaches elements designed to store an actual repair signature for the memories (col. 11, lines 26-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the elements of Weiss shown in Fig. 6 into a repair data container such as the one disclosed by Anand. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because it has been held that integrating together a plurality of pieces involves only routine skill in the art. *In re Larson* 144 USPQ 347 (CCPA 1965).

As per claim 37:

Weiss teaches a machine readable medium that stores data representing an integrated circuit, comprising:

- two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells (Fig. 6, elements 700-715);
- a processor containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each memory (col. 16, lines 12-20).

Not explicitly disclosed by Weiss is a repair data container to store an actual repair signature for each memory having one or more defective memory cells and a dummy repair signature for each memory with no defective memory cells. However, Anand in an analogous art teaches a repair data container (Fig. 1, element 11), and Weiss teaches elements designed to store an actual repair signature for each memory having one or more defective memory cells detected during fault testing (col. 11, lines 26-33)

and a dummy repair signature for each memory with no defective memory cells (col. 11, lines 43-46).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the elements of Weiss shown in Fig. 6 into a repair data container such as the one disclosed by Anand. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because it has been held that integrating together a plurality of pieces involves only routine skill in the art. *In re Larson* 144 USPQ 347 (CCPA 1965).

7. Claims 22-26 and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand.

As per claim 22:

Anand teaches an apparatus, comprising:

- a fuse box to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor (Fig. 1, element 11).

Not explicitly disclosed by Anand is a first processor containing logic configured to test and repair two or more memories connected to that first processor; and a second processor containing logic configured to test and repair two or more memories connected to that second processor. However, Anand teaches that an integrated circuit for testing and repairing at least two memories connected thereto (Fig. 1, element 10).

However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement a second processor along with a first processor to test and repair respective memories since it is suggested by Anand in col. 3, line 67-col. 4, line 2.

As per claim 23:

Anand teaches the apparatus of claim 22, wherein the first processor contains logic configured to decompress an amount of bits making up the concatenated repair signature (Fig. 1, element 14).

As per claim 24:

Anand teaches the apparatus of claim 22, further comprising: an amount of non-volatile fuses contained in the fuse box to provide actual repair capability for only a subset of all of the memories that share the fuse box (col. 3, lines 27-28).

As per claim 25:

Anand teaches the apparatus of claim 22, wherein the fuse box is located external to the memories (see Fig. 1).

As per claim 26:

Anand teaches the apparatus of claim 22, wherein the processors and the fuse box are embedded on a single chip (see Fig. 1).

As per claim 33:

Anand teaches a machine readable medium that stores data representing an integrated circuit, comprising:

- a fuse box to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor (Fig. 1, element 11).

Not explicitly disclosed by Anand is a first processor containing logic configured to test and repair two or more memories connected to that first processor; and a second processor containing logic configured to test and repair two or more memories connected to that second processor. However, Anand teaches that an integrated circuit for testing and repairing at least two memories connected thereto (Fig. 1, element 10).

However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement a second processor along with a first processor to test and repair respective memories since it is suggested by Anand in col. 3, line 67-col. 4, line 2.

8. Claims 34, 36, and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Rona (US Pat. 5,350,940).

As per claim 34:

Anand teaches the machine-readable medium of claim 32 above. Not explicitly disclosed by Anand is wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the fuse box and the processors. However, Rona teaches fabrication of semiconductors using lithographic masks (col. 8, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lithographic mask. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that fabrication using lithographic masks is well known (col. 8, lines 35-38).

As per claim 36:

Weiss and Anand teach the machine-readable medium of claim 35 above. Not explicitly disclosed is wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the repair data container and the two or more memories. However, Rona teaches fabrication of semiconductors using lithographic masks (col. 8, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lithographic mask. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that fabrication using lithographic masks is well known (col. 8, lines 35-38).

As per claim 38:

Weiss and Anand teach the machine-readable medium of claim 37 above. Not explicitly disclosed is wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the repair data container, the processor, and the two or more

memories. However, Rona teaches fabrication of semiconductors using lithographic masks (col. 8, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lithographic mask. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that fabrication using lithographic masks is well known (col. 8, lines 35-38).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Chen et al (USP 6603690);

Shimizu et al (USP 6822912);

Ouellette et al ("Shared fuse macro for multiple embedded memory devices with redundancy").

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steve Nguyen
Examiner
Art Unit 2138

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100